DECLARATION & POWER OF ATTORNEY

As a below-named inventor, I hereby declare that:

My correct residence, post office address and citizenship are stated below next to my name.

I believe myself to be the original, first and sole inventor of the subject matter which is disclosed

and claimed and for which a patent is sought on the invention entitled:

"METHOD AND APPARATUS FOR BORDER NODE

BEHAVIOR ON A FULL-DUPLEX BUS"

The specification of this subject matter:

☐   is attached hereto.

x   was filed on January 18, 2000;

I hereby state that I have reviewed and understand the contents of the above identified patent application, including the claims, as amended by any amendment(s) referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with 37 C.F.R. §1.56(a).

I hereby claim foreign priority benefits under 35 U.S.C. §119 (a)-(d) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)			Priority Claimed	
Number	Country	Month/Day/Year Filed	Yes	No
Number	Country	Month/Day/Year Filed	Yes	No
Number	Country	Month/Day/Year Filed	Yes	No

I hereby claim the benefit under 35 U.S.C. §119(e) of any United States provisional application(s) listed below:

Application Number	Filing Date
Application Number	Filing Date

I hereby claim the benefit under 35 U.S.C. §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in these prior United States application(s) in the manner provided by 35 U.S.C. §112, I acknowledge the duty to disclose material information as defined in 37 C.F.R. §1.56(a) which occurred between the filing date of the prior application(s) and the national or PCT international filing date of this application.

Application No.	Filing Date	Status (Issued, Pending, Abandoned)
Application No.	Filing Date	Status (Issued, Pending, Abandoned)
Application No.	Filing Date	Status (Issued, Pending, Abandoned)
Application No.	Filing Date	Status (Issued, Pending, Abandoned)

I hereby appoint Kenneth D'Alessandro, Registration No. 29,144; Timothy Brisson, Registration No.: 44,046; Michael Brandt, Registration No.: 39,119; Robert Hall, Registration No.: 39,209, Jonathan Velasco, Registration No.: 42,200, Michael Kerr, Registration No.: 42,722 and Victor Gallo, Registration No.: 41,768, as attorneys of record with full power of substitution and revocation, to prosecute this application and transact all business in the United States Patent and Trademark Office connected therewith, and certifies that it is the assignee of the entire right, title and interest in the patent application identified above by virtue of an assignment, a copy of which is attached, from the inventor(s) of the patent application identified above.

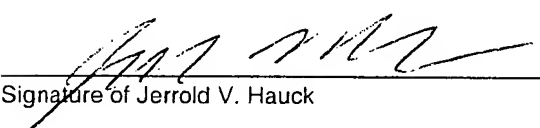Please send all correspondence and direct all telephone calls to:

Timothy A. Brisson
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P.O. Box 6149
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I, the undersigned, declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing therefrom.

FULL NAME OF INVENTOR 1	FIRST Name	MIDDLE Initial(s)	LAST Name	
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FULL NAME OF INVENTOR 2	FIRST Name	MIDDLE Initial(s)	LAST Name	
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	9, Pitch and Pay Lane, Sneyd Park	Bristol	United Kingdom	BS91NH

I further declare that all statements made herein of my own knowledge are true and that all statements made upon information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.
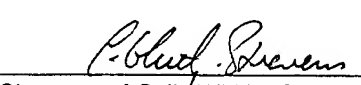
_____   2/8/2000
Signature of Jerrold V. Hauck   Date

_____   FEB 11 2000
Signature of Colin Whitby-Strevens   Date

SCHEDULE A

Patents, Patent Applications and Inventions

Descriptive Invention Title	Invention Date	US Filing Date	Inventor(s)	Textual Status	Docket Number	Serial Number
Method for optimizing acknowledge packet rate	6/1/97	7/21/98	Bill Duckwall	Allowed	ZAY-001	09/121,616
Pipelined arbitration for a bus using dual phases	Q3 '98 ?	11/5/99	Mike Teener	Filed	ZAY-99-012	09/435,134
P1394a Loop Breaking	3/12/99 - 3/16/99	7/9/99	Jerry Hauck Colin Whitby-Stevens	Filed	ZAY-002	09/350,583
P1394b Loop Breaking	4/27/99	11/5/99	Jerry Hauck Colin Whitby-Stevens	Filed	ZAY-99-018	
P1394b Automatic Cross-over of TPA/TPB	4/16/99	4/21/00	Colin Whitby-Stevens	Filed	ZAY-00-019	09/557,073
Dynamic CSR ROM	6/23/98	11/1/99	Steve Brown	Filed	ZAY-99-027	09/431,409
Link Driver Architecture - Link Configuration	3/2/98	11/1/99	Steve Brown	Filed	ZAY-99-029	09/431,703
Device communication path construction	10/1/97	11/2/99	Erik Staats	Filed	ZAY-99-034	09/432,915
Distributed device control over multiple transports	8/1/97	11/1/99	Erik Staats	Filed	ZAY-99-037	09/431,704
Bridging of distributed device control through multiple transports	8/1/97	11/2/99	Erik Staats	Filed	ZAY-99-038	09/432,997
AV/C over multiple transports	1/1/99	2/16/00	Erik Staats	Filed	ZAY-99-039	
Allocation of IDs for AV/C entities	8/1/98	11/2/99	Erik Staats	Filed	ZAY-99-041	09/432,872

Descriptive Invention Title	Invention Date	US Filing Date	Inventor(s)	Textual Status	Docket Number	Serial Number
Generic container mechanism for implementing AV/C descriptors	10/1/98	10/28/99	Erik Staats	Filed	ZAY-99-044	09/429,233
Jitter Test Patterns	4/20/99	4/21/00	Colin Whitby-Strevens	Filed		
Detection of a P1394b Hybrid Bus	6/11/99	1/18/00	Colin Whitby-Strevens Jerry Hauck	Filed	ZAY-99-054	
Dual phase arbitration without timers	3/10/99	3/31/00	Mike Teener David Wooten	Filed	1662-16900	
Protecting D/S Clouds from Beta Packets	8/18/99	2/17/00	Jerry Hauck	Filed	ZAY-99-062	
Link Driver Architecture - Node presentation	8/1/97	11/2/99	Steve Brown	Filed	ZAY-99-065	09/432,869
Accelerated Speed Signal Detection	4/29/99	11/16/99	Bill Duckwall	Filed	ZAY-99-067	
P1394b Loop Breaking Refined	6/14/00		David Wooten Jerry Hauck Colin Whitby-Strevens			
Fly-by and ack-accelerated arbitration for broadcasts	7/13/99		Jerry Hauck Prashant Kanhere Bill Duckwall			
Automatic Avoidance of >62 Node Topologies	3/26/99		Colin Whitby-Strevens			
Optimized P1394a Gap Calculations when Pinging	3/10/99		Jerry Hauck			

Descriptive Invention Title	Invention Date	US Filing Date	Inventor(s)	Textual Status	Docket Number	Serial Number
Methods for interoperability with legacy S100 PHYs	10/20/98		Bill Duckwall			
Dynamic compensation for Link's GRANT to Data Delay	7/5/99		Bill Duckwall			
PHY cable event			Steve Brown			
Generational resource locking mechanism			Erik Staats			
Streaming data flow control with error recovery			Erik Staats			
Hierarchical references to AV/C entries			Erik Staats			
Optimizing of Disparity Control Phases	6/17/99		Jerry Hauck Colin Whitby-Stevens			
P1394b Legacy Request	5/16/99		Jerry Hauck			
PHY ID 62 reserved for root	7/30/99		Colin Whitby-Stevens			
Selection and Identification of Preferred Border	7/14/99		Colin Whitby-Stevens Jerry Hauck			
P1394b Scalable Bus Busy Indicator	6/17/99		Jerry Hauck Colin Whitby-Stevens			
Restoring Local Root as BOSS	5/21/99		Jerry Hauck			
BOSS vs OK to grant	5/19/99		Jerry Hauck			
Freeing Beta-Only Nodes of Gap Timers	5/13/99		Jerry Hauck			

Descriptive Invention Title	Invention Date	US Filing Date	Inventor(s)	Textual Status	Docket Number	Serial Number
Improved Jitter Test Patterns	9/8/99		Colin Whitby-Stevens			